EXHIBIT 4

EXPEDITED PROCEDURE
Group Art Unit: 2116
Docket No.: SCEI 3.0-070

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Suzuoki et al.	::
Application No.: 10/959,700	:: Group Art Unit: 2116
Filed: October 5, 2004	:: Examiner: T. C. Lee
For: POWER MANAGEMENT IN A PROCESSING ENVIRONMENT	::

AMENDMENT PURSUANT TO 37 C.F.R. § 1.116

MS RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the final Office Action dated June 1, 2007, finally rejecting claims 1, 3-7, 9-14, 16-23, 25-30 and 32-34, please amend the above-identified U.S. patent application as follows:

IN THE CLAIMS

1. (currently amended) A method for performing power management, the method comprising the steps of:

monitoring a rate of execution of instructions by a processor to determine a heat level for the processor; and

estimating a power consumption rate as a function of the heat level according to the monitored instruction execution rate so that processing by the processor is controllable according to the power consumption rate based on the heat level;

wherein the rate of execution is monitored based on a rate of fetching instructions for execution, wherein the instructions include instructions having different types.

2. (cancelled)

3. (currently amended) The method of claim 1, wherein determining the ~~estimating step estimates a~~ heat level for the processor is done as a function of instruction count values for each of the different types of instruction being executed.

4. (previously presented) The method of claim 1, wherein the different types of instructions include a floating point instruction and an integer instruction.

5. (previously presented) The method of claim 1, wherein the different types of instructions include a vector floating point instruction, a vector integer instruction, a scalar floating point instruction and a scalar integer instruction.

6. (cancelled)

7. (currently amended) A method for performing power management, the method comprising the steps of:

determining power information based on a rate of execution of instructions by a first processor; ~~and~~

sending the power information to a second processor; and

estimating a rate of power consumption by the second processor as a function of the determined power information so that processing by the first processor is controllable according to the rate of power consumption;

wherein the instructions are of different types, and the power information is determined by counting the number of each of the respective types of instructions being executed by the first processor.

8. (cancelled)

9. (previously presented) The method of claim 7, wherein the different types of instructions include a floating point instruction and an integer instruction.

10. (previously presented) The method of claim 7, wherein the different types of instructions include a vector floating point instruction, a vector integer instruction, a scalar floating point instruction and a scalar integer instruction.

11. (cancelled)

12. (currently amended) The method of claim ~~11~~7, wherein the second processor controls the first processor to reduce energy usage if the estimated energy usage is above a predefined level.

13. (original) The method of claim 12, wherein the second processor puts the first processor into an idle state.

14. (currently amended) Apparatus performing power management, the apparatus comprising:

a first processor; ~~and~~

a second processor; and

a monitoring circuit operable to generate power information based on a rate of execution of instructions by the first processor;

wherein the first processor is operable to send the power information to the second processor, the second processor is operable to estimate a rate of power consumption by the first processor, wherein the rate of execution is represented by a rate of fetching instructions for execution, the instructions include instructions having different types and the power information includes counts of each of the different types of instructions being fetched for execution.

15. (cancelled)

16. (previously presented) The apparatus of claim 14, wherein the different types of instructions include a floating point instruction and an integer instruction.

17. (previously presented) The apparatus of claim 14, wherein the different types of instructions include a vector floating point instruction, a vector integer instruction, a scalar floating point instruction and a scalar integer instruction.

18. (previously presented) The apparatus of claim 14, wherein the monitoring circuit includes counters for maintaining the counts of each of the different types of instructions.

19. (cancelled)

20. (currently amended) The apparatus of claim ~~19~~14, wherein the second processor is operable to estimate a heat level corresponding to the estimated rate of power consumption.

21. (previously presented) A processing element for performing power management, the processing element comprising:

a first processing unit;

a number of attached processing units, at least one attached processing unit having a monitoring circuit operable to accumulate power information related to a rate at which instructions are executed therein;

wherein the at least one attached processing unit is operable to send the accumulated power information to the first processing unit, and the first processing unit is operable to determine a rate of power consumption from the accumulated power information;

wherein the instructions include instructions having different types, and wherein the accumulated power information includes data representing counts for how many instructions of the different types of instructions have been executed.

22. (original) The processing element of claim 21, wherein the first processing unit is operable to reduce an energy usage of the at least one attached processing unit if the determined power consumption for that attached processing unit is above a predefined value.

23. (original) The processing element of claim 21, wherein the first processing unit is operable to reduce an energy usage of that attached processing unit by causing that attached processing unit to enter an idle state.

24. (cancelled)

25. (previously presented) The processing element of claim 21, wherein the different types of instructions include a floating point instruction and an integer instruction.

26. (previously presented) The processing element of claim 21, wherein the different types of instructions include a vector floating point instruction, a vector integer instruction, a scalar floating point instruction and a scalar integer instruction.

27. (original) The processing element of claim 21, wherein the first processing unit is operable to estimate a heat level corresponding to the determined rate of power consumption.

28. (previously presented) A processing environment comprising:

a first processing unit;

a number of additional processing units each having a monitoring circuit operable to generate power information based on a rate at which instructions are executed by the respective additional processing unit;

wherein the additional processing units are operable to send power information to the first processing unit, the first processing unit being operable to monitor a rate of power consumption of the additional processing units based on the sent power information;

wherein the instructions include instructions having different types and the accumulated power information includes data representing counts of each of the different types of instructions that are executed.

29. (original) The processing environment of claim 28, wherein the first processing unit reduces the rate of power consumption of at least one of the attached processing units when the rate of power consumption is above a predefined value.

30. (original) The processing environment of claim 28, wherein the first processing unit reduces the power consumption of the at least one attached processing unit by causing that attached processing unit to enter an idle state.

31. (cancelled)

32. (previously presented) The processing environment of claim 28, wherein the different types of instructions include a floating point instruction and an integer instruction.

33. (previously presented) The processing environment of claim 28, wherein the different types of instructions include a vector floating point instruction, a vector integer instruction, a scalar floating point instruction and a scalar integer instruction.

34. (original) The processing environment of claim 28, wherein the first processing unit further estimates a heat level based on the monitored rate of power consumption.

REMARKS/ARGUMENTS

The present amendment is responsive to the final Office Action dated June 1, 2007. Claims 1, 3, 7, 12, 14 and 20 have been amended. Claims 6, 11 and 19 have been cancelled. Claims 2, 8, 15, 24 and 31 were previously cancelled. Thus, claims 1, 3-5, 7, 9-10, 12-14, 16-18, 20-23, 25-30 and 32-34 are again presented for consideration by the Examiner in view of the following comments. A Request for Continued Examination is also submitted herewith.

Reexamination and reconsideration of the above-identified application, pursuant to and consistent with 37 C.F.R. § 1.116, and in light of the amendments and remarks that follow, are respectfully requested. Because the present claims are believed to be in condition for allowance over the cited art, good cause exists for the entry of this amendment in accordance with 37 C.F.R. § 1.116.

Prior to addressing the substance of the Office Action, applicant would like to note that there that there are a few pending applications for the same assignee which contain similar subject matter to the instant application. The applications are U.S. Patent Application No. 10/812,177 ("the '177 application"), U.S. Patent Application No. 10/812,155 ("the '155 application") and U.S. Patent Application No. 10/801,308 ("the '308 application").

The '177 application received an Office Action from Examiner Alhija in Group Art Unit 2128 dated May 3, 2007. An amendment was filed in response on June 21, 2007.

The '155 application received a final Office Action from Examiner Stoynov in Group Art Unit 2116 dated June 13, 2007. A reply to the final Office Action has not been filed as of today's date.

The '308 application has yet to receive an Office Action on the merits.

In view of 37 C.F.R. § 1.56, § 2001.06(b) of the Manual of Patent Examining Procedure, and the fact that different Examiner are assigned to the '177 and '155 applications, applicants submit the following herewith:

(1) a copy of the most recent Office Action in the '177 application;

(2) a copy of the claims as presently presented in the most recent amendment filed in the '177 application;

(3) a copy of the most recent Office Action in the '155 application;

(4) a copy of the claims as presently presented in the most recent amendment filed in the '155 application; and

(5) a copy of the claims as originally filed in the '308 application.

Returning to the instant application, claims 1, 3-7, 9-14, 16-23, 25-30 and 32-34 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 7,096,145 ("*Orenstien*"). Applicants respectfully traverse the rejection. Claims 1, 7, 14, 21 and 28 are independent.

Turning to *Orenstien*, the reference discloses a processing system having a microprocessor 102 which includes a "thermal control system" 104, as shown in FIG. 1. As described in the patent, the thermal control system 104 includes a power usage monitoring unit 108 and a throttle control unit 110. (*See* col.3, ll.19-21.) Various examples are given as to how monitor power usage. *Orenstien* explains as follows:

> For example, one counter monitored by the power usage monitoring unit 108 may be configured to count the number of floating point operations performed by the microprocessor during a sampling time period. Another counter may be configured to count the number of cache memory accesses occurring in the microprocessor, data from which may be used to estimate the amount of power consumed by the microprocessor. The number of instructions decoded by the decoder may also be another activity monitored by the power usage monitoring unit 104 via some sort of counter mechanism. It should be understood that the present invention may be implemented by monitoring any other suitable activities occurring within the microprocessor and is limited to examples specified herein.
>
> (Col.3, ll.44-57.)

As presently understood by applicants, *Orenstien* focuses on power monitoring and managing the microprocessor in view of the power. *Orenstien* discusses in the background "thermal diode based throttling" but indicates that the use of thermal diodes to protect a microprocessor from overheating is disadvantageous as it "creates a non-deterministic behavior since each chip has a different thermal response, leakage current, etc." (Col.1, ll.55-57.) *Orenstien* goes on to state that:

> One problem associated with the conventional microprocessors using thermal diodes is that they do not provide deterministic results from one system to another system. For example, because the temperature of the die is measured using thermal diodes, various factors may affect the temperature measurement and the performance of the system. In addition, each microprocessor is fabricated with slightly different parameters such as static power level, temperature responses, etc. and slightly different behavior such as heat sink capability, quality, etc. As a result, the performance of different microprocessors measured using the same benchmark program under similar condition will provide different performance results. Because the timing of when throttling is activated is

different from one microprocessor to another, the behavior of each microprocessor will be non-deterministic, resulting in one microprocessor performing better than another microprocessor. To avoid high junction temperature for all microprocessors, a higher margin value may need to be assigned so that throttling can be timely activated in less sensitive microprocessors, which results in a loss of performance. Another problem associated with non-deterministic behavior is the added complexity in validation and system debugging, typically performed by OEM and IT managers of large companies purchasing a large amount of portable computer systems, such as notebooks.

(Col.6, ll.28-52.)

Orenstien then distinguishes its invention from such temperature or heat-based systems by stating:

In contrast, a microprocessor implementing the thermal control system according to one embodiment provides a deterministic behavior. This means that the performance of the microprocessor does not depend on chance but rather can be replicated one run after another. This means that when the same application program is executed on different motherboards, they will generate the same count value and have the same throttling behavior and performance. Advantageously, by using the same maximum allowed power usage value and weighting factor values, the scheme taught by the present invention enables the throttling mechanism to be activated in a deterministic manner.

(Col.6, ll.53-64.)

As noted above, claims 1, 3, 7 and 14 have been amended to clarify the invention. Independent claim 1 was amended to include the limitations of dependent claim 6. Independent claim 7 was amended to include the limitations of dependent claim 11. And independent claim 14 was amended to include the limitations of claim 19. For the sake of brevity, the claims are not reproduced below.

With regard to claims 1 and 3, the Office Action cited to a column 2, lines 17-32 of *Orenstien* to address the limitations of claim 3 and (now cancelled) claim 6. The cited section of *Orenstien* states:

A thermal control system is described. In one embodiment, a thermal control system is provided that uses a **digital power monitoring for thermal control** in computer systems. The digital monitoring of power is configured **to estimate an amount of power used by a microprocessor**. Based on the estimated power usage, the thermal control system controls the activation and deactivation of throttling mechanism to avoid unsafe junction temperature that may cause system degradation or that exceeds system specification.

It has been found than the amount of power consumed by a microprocessor during a time interval is related to junction temperature (Tj) on the die of the microprocessor. In other words, when the microprocessor within a computer

> system consumes relatively a large amount of power for a period of time, this may indicate that the microprocessor is operating at relatively high temperature.
>
> (Col.2, ll.17-32, emphasis added.)

Applicants respectfully submit that nothing in the cited portion or elsewhere in *Orenstien* discloses determining a heat level, and the reference clearly does not disclose or suggest determining a heat level as a function of instruction count values for the different types of executed instructions as claimed.

With regard to independent claims 7 and 14 and the features incorporated from claims 11 and 19, the Office Action asserts that *Orenstien* discloses a second processor that is operable to estimate a rate of power consumption by a first processor. Applicants respectfully disagree. The Office Action points to element 108 of *Orenstien* as the second processor and cites to a few lines in the specification which state:

> In general, there are a number of functional units within a microprocessor, each of which consumes different amount of power. Accordingly, by counting the number of times certain functional units are activated during a defined time period, the amount of power consumed by the microprocessor during that time period may be estimated.
>
> (Col.3, ll.32-37.)

Notwithstanding the Office Action's assertions, applicants submit that *Orenstien* clearly does not disclose multiple processors. Element 108 is the power usage monitoring unit, which is a subcomponent of the thermal control system 104, which itself is a part of microprocessor 102. (*See* col.2, ll.55-57 and col.3, ll.19-21.)

In fact, in one embodiment, "the power usage monitoring unit **104 is embodied in the form of software code** such as micro-code executed periodically within the microprocessor to estimate power consumption based on the number of occurrences of various activities performed in the microprocessor." (Col.3, ll.21-26, emphasis added.) Thus, in this embodiment, element 104 and its subcomponents are arguable purely software and cannot be a processor.

Nothing in *Orenstien* suggests that the element 108 or the element 104 is intended to be a processor as claimed. Thus, applicants submit that it is erroneous to construe element 108, element 104 or another such subcomponent as a processor. This is further supported by applicants' own specification, which provides numerous examples of processors therein.

Independent claims 21 and 28 are now addressed together. Claim 21 requires a number of attached processing units in addition to the first processing unit. And claim 28

requires a number of additional processing units in addition to the first processing unit. As discussed above with regard to claims 7 and 14, *Orenstien* simply does not disclose a multiprocessor arrangement, and does not teach or otherwise suggest the various processors operating as claimed.

Applicants also note that the claimed attached processing units are a specific type of processor as disclosed in applicants' specification, and this cannot be ignored when analyzing the teachings of the cited art. Applicants respectfully submit that *Orenstien* simply does not disclose such structures as claimed.

Thus, for at least the reasons presented above, *Orenstien* does not anticipate independent claims 1, 7, 14, 21 and 28.

Claims 3-5, 9-10, 12-13, 16-18, 20, 22-23, 25-27, 29-30 and 32-34 depend from independent claims 1, 7, 14, 21 and 28, respectively, and contain all the limitations thereof. For at least this reason, applicants submit that the subject dependent claims are likewise in condition for allowance.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that the Examiner telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which he might have. If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

Dated: August 24, 2007

Respectfully submitted,

By _____

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